Metrol. Meas. Syst., Vol. XVIII (2011), No. 4, pp. 631-644

PAN POLSKA AKADEMIA NAUK

METROLOGY AND MEASUREMENT SYSTEMS

Index 330930, ISSN 0860-8229

www.metrology.pg.gda.pl

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64 CHANNEL NEURAL RECORDING AMPLIFIER WITH TUNABLE BANDWIDTH IN 180 nm CMOS TECHNOLOGY

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Abstract

This paper presents the design and measurements of low-noise multichannel front-end electronics for recording extra-cellular neuronal signals using microelectrode arrays. The integrated circuit contains 64 readout channels and is fabricated in CMOS 180 nm technology. A single readout channel is built of an AC coupling circuit at the input, a low-noise preamplifier, a band-pass filter and a second amplifier. In order to reduce the number of output lines, the 64 analog signals from readout channels are multiplexed to a single output by an analog multiplexer. The chip is optimized for low noise and good matching performance and has the possibility of pass-band tuning. The low cut-off frequency can be tuned in the 1 Hz – 60 Hz range while the high cut-off frequency can be tuned in the 3.5 kHz - 15 kHz range. For the nominal gain setting at 44 dB and power dissipation per single channel of 220 μW, the equivalent input noise is in the range from 6 μV - 11 μV rms depending on the band-pass filter settings. The chip has good uniformity concerning the spread of its electrical parameters from channel to channel. The spread of the gain calculated as standard deviation to mean value is about 4.4% and the spread of the low cut-off frequency set at 1.6 Hz is only 0.07 Hz. The chip occupies 5×2.3 mm^2 of silicon area. To our knowledge, our solution is the first reported multichannel recording system which allows to set in each recording channel the low cut-off frequency within a single Hz with a small spread of this parameter from channel to channel. The first recordings of action potentials from the thalamus of the rat under urethane anesthesia are presented.

Keywords: neurobiological measurements, low noise amplifier, neural recording, band-pass filter, multichannel ASIC.

1. Introduction

Frontiers of neurobiological and pharmacological experiments need multi-channel readout systems for simultaneous recording of extra-cellular signals from many neuronal cells. Since, technology has made a large progress, combining the multichannel biocompatible recording electrodes with integrated electronics is possible and permits to build systems for both in vivo and in vitro experiments. These systems cover research with a broad range of interests. Some of them aim to find answers to principal questions: how a complicated neuronal system, like the retina or brain, codes and processes information [1-4]. There are also experiments connected with cultured neuronal networks, which emerged as a powerful tool in the assessment of acute neuropharmacological effects of both known and unknown agents [5-7].

Article history: received on July 4, 2011; accepted on Oct. 18, 2011; available online on Dec. 12, 2011.

In order to characterize large neuronal systems one needs to collect information regarding the mutual relations in neighboring cells. Thus a system capable of recording signals simultaneously from many recording sites is necessary. Therefore, a lot of groups are carrying intensive research to develop a low power, low-noise Application Specific Integrated Circuit (ASIC) for extracellular recording [8-13]. The main advantage of the integrated circuits are the size of the final system and its low power consumption, what with combined multichannel recording electrodes can increase the spatial resolution and thereby provide a robust measure of neural activity.

Based on our experience in design and practical applications of ASICs for recording systems comprising hundreds of electrodes [13-19], we propose a novel 64-channel ASIC. Our priority was proper ASIC operation in a multichannel system in the low frequency range to record LFP (Local Field Potentials) signals and also the neuronal spikes. Thus, we concentrated on:

- good uniformity of low corner frequency (of about 1 Hz),
- low power consumption,
- low-noise performance,
- multiplexing the recorded data at the output without any additional digital noise in the overall input referred noise.

The paper is organized as follows. Section 2 describes the ASIC architecture. The measurements of the multi-channel IC are presented in Section 3, while the results of neurobiological experiments are presented in Section 4. Finally, Section 5 contains a summary.

2. Chip Architecture

The ASIC comprises three basic blocks: 64 AC-coupled circuits at the inputs, 64 analog channels with the amplifiers and filters, and an analog 64:1 multiplexer (see Fig. 1). It is fabricated in CMOS 180 nm technology and occupies 5 x 2.3 mm^2 of silicon area.

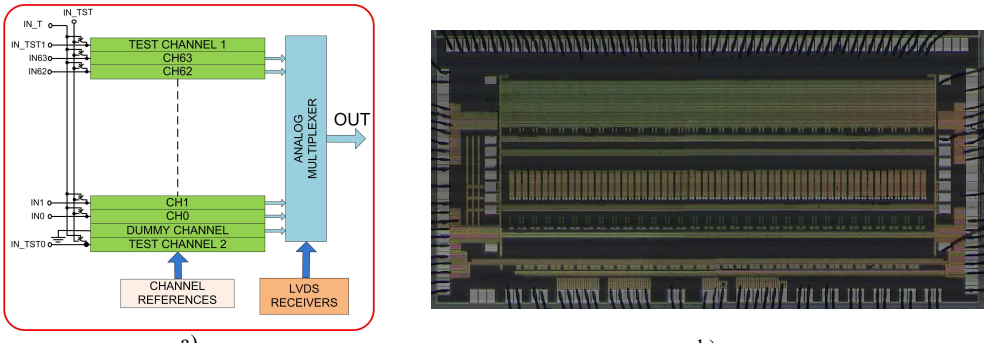


Fig. 1. Multichannel recording ASIC: a) block diagram, b) photo of a 64-channel chip: input pads are at the top side, control and output pads are at the bottom side, power supply and test pads are on the left and right side.

The 64 analog channels amplify and filter small amplitude biopotential signals, which are typically in the range from tens to hundreds of μV with the frequency spectrum from a few Hz to a few kHz. The signals are recorded with respect to a common reference electrode INREF immersed in a physiological saline solution. The low and the high cut-off frequencies of the channel are controlled by external signals. The signals from the 64 channels are

sampled at the same moment and subsequently multiplexed through the analog multiplexer to the output buffer.

2.1. Architecture of the analog readout channel

Since the readout channel is part of the multichannel system and records small amplitude input signals, one has to take into account requirements concerning uniformity of analog parameters in all 64 channels, low-noise performance and also power limitation. The proposed architecture of a single readout channel is shown in Fig. 2. It consists of three main sections: AC coupled input preamplifier, band-pass filter stage with AC coupled output and a second amplifier.

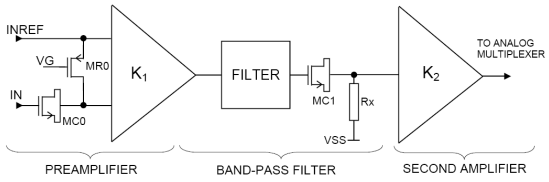


Fig. 2. Simplified block diagram of a single readout channel.

2.2. AC coupling circuits

Using AC coupling in the readout channel suppresses the DC offset propagation through the entire signal path (in this case the total gain is about 44 dB) and improves the uniformity of the analog parameters in the multichannel system. Additionally the AC coupling circuits work as high-pass filters and suppress the low frequency 1/f noise generated in MOS transistors.

The AC coupling circuits are used twice in the readout channel:

- at the input of the preamplifier (transistors MC0-MR0) to cut off the offsets generated by the interface between electrodes and biological cells,
- at the output of the filter stage (elements MC1-Rx) to cut off the offsets generated by the preamplifier and filter.

The high value of input capacitors MC0 (with effective capacitance C_{MC0} = 165 pF) is realised using MOS transistors of W_{MC0}/L_{MC0} = 400 μm/50 μm biased in the strong inversion region. The MR0 is formed as an array of six PMOS transistors with W_{MR0}/L_{MR0} = 0.4 μm/50 μm each, connected in series and working in the linear region. By changing the gate voltage VG of the transistor MR0 (see Fig. 2) one controls the low cut-off frequency at the preamplifier input.

The second AC coupling has also a MOS capacitor MC1 (with a much lower area W_{MC1}/L_{MC1} = 60 μm/29.5 μm) and the effective resistance Rx based on two current sources as it is described in [19]. The low cut-off frequency of this circuit is much below a single Hz.

2.3. Low-noise preamplifier

The scheme of a low-noise preamplifier is shown in Fig. 3. It is based on a transconductance amplifier which follows the AC coupling circuit (MR0 and MC0 transistors) and the source follower (MSF0, MSF1 and MSF2 transistors). The CMOS 180 nm technology used provides two types of the capacitors: MIM (metal-insulator-metal) and

capacitors based on the MOS transistors. Nevertheless if a MOS transistor is biased in the strong inversion region it occupies an area six times smaller than a MIM capacitor of the same capacitance value. In order to shift transistors MC0 operation region into strong inversion, the source follower MSF0-MSF2 is used. The drawback of this solution is that this block consumes a significant amount of power and is the source of an additional noise at the input.

The capacitance C_0 = 1 pF in the feedback of the differential pair limits the preamplifier bandwidth to 440 kHz. The current consumption of this stage is 95 µA and its gain is 38 dB. The transistor dimensions used in the preamplifier together with their operation region are shown in Table 1.

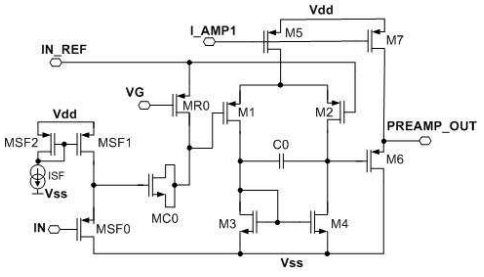


Fig. 3. Simplified scheme of the preamplifier.

Table 1. Parameters of the main components of the preamplifier.

Component	Parameter	g_m/ I_d[V^{-1}]	Operating Region*
MSF0	350 µm/4 µm	8.5	MI
MR0	0.4 µm/300 µm	-	WI
MC0	400 µm/50 µm	-	SI
C0	1 pF	-	-
M1, M2	175 µm/0.5 µm	22.1	WI
M3, M4	20 µm/2 µm	17.6	MI
M5, M7	100 µm/5 µm	4.5	MI
M6	10 µm/5 µm	13.4	MI

* Abbreviations used: WI – weak inversion, MI – moderate inversion, SI – strong inversion.

Small signal analysis gives the transfer function of the preamplifier:

$$K_0(s) \approx K_0 \frac{\frac{s}{z_0}}{(1+\frac{s}{p_0})(1+\frac{s}{p_1})}, \tag{1}$$

where K_0, z_0, p_0 and p_1 are given by:

$$K_0 \approx g_{mM2} r_{dsM24},\ z_0 = \frac{1}{r_{dsMR0} C_{MC0}},\ p_0 = \frac{1}{r_{dsMR0} C_{MC0}},\ p_1 = \frac{1}{2 r_{dsM24} C_0}, \tag{2-5}$$

where: $r_{dsM24} = r_{dsM2} || r_{dsM4}$ is a parallel connection of small signal drain-source resistances of the M2 and M4 transistors, g_{mM2} is the transconductance of the M2 transistor, r_{dsMR0} is the small-signal resistance of the MR0 transistor working in the linear region, C_{MC0} is the effective gate capacitance of the MC0 transistor, and C_0 is a capacitance in the feedback circuit of the differential amplifier.

Because of low amplitudes of input signals the amplifier has to be optimized for low-noise performance. The total noise of the preamplifier is the sum of three main components:

- noise of the differential amplifier M1-M5,
- noise of the AC coupling circuit MC0-MR0,
- noise of the source follower MSF0-MSF2 transistors.

In the noise consideration both thermal and flicker noise contributions have to be taken into account. Thus, for 1/f noise we can write a formula for the preamplifier:

$$\frac{\overline{dv^2_{1/f\_dif}}}{df} = \frac{2K_{fp}}{C_{ox} W_{M1} L_{M1}} \left(1 + \frac{\mu_n K_{fn} L^2_{M1}}{\mu_p K_{fp} L^2_{M3}}\right) \frac{1}{f}, \tag{6}$$

where K_{fn}, K_{fp} are flicker noise constants for NMOS and PMOS transistors, C_{ox} is the oxide capacitance per gate area, W_1 is the width of the transistor M1 gate, L_1, L_3 are lengths of the transistors M1 and M3 gate, μ_n, μ_p is the carrier mobility in the NMOS and PMOS channel, and f is the frequency.

Then the thermal noise contribution of the first stage to the overall input equivalent noise is given by:

$$\frac{\overline{dv_{th\_dif}^2}}{df} = \frac{16}{3}\frac{kT}{g_{mM1}}\left(1+\frac{g_{mM3}}{g_{mM1}}\right). \tag{7}$$

As discussed previously the AC-coupling circuit MC0-MR0 should not be neglected in the overall input equivalent noise calculations. Thus it may be written:

$$\frac{\overline{dv_{th\_AC}^2}}{df} = \frac{4kTr_{dsMR0}}{1+\left(\frac{f}{f_0}\right)^2}, \tag{8}$$

where:

$$f_0 = (2\pi C_{MC0} r_{dsMR0})^{-1}. \tag{9}$$

Taking the MSF0-MSF2 source follower into consideration, its output equivalent current noise is given by:

$$\frac{\overline{di_{n\_SF}^2}}{df} = \frac{\overline{di_{n\_MSF0}^2}}{df} + \frac{\overline{di_{n\_MSF1}^2}}{df} + B^2\frac{\overline{di_{n\_MSF2}^2}}{df}, \tag{10}$$

where B is the multiplication factor of the MSF1-MSF2 current mirror, $\overline{di_{n\_MSF0}^2}/df$, $\overline{di_{n\_MSF1}^2}/df$, $\overline{di_{n\_MSF2}^2}/df$ are power spectral densities of the current noise in transistors MSF0, MSF1 and MSF2.

Taking into account both thermal and flicker noise contributions we obtain the input-referred voltage noise contribution of the considered source follower:

$$\frac{\overline{dv_{th\_SF}^2}}{df} = 4kT\frac{2}{3}\left(\frac{1}{g_{mMSF0}} + \frac{g_{mMSF1}}{g_{mMSF0}^2} + B^2\frac{g_{mMSF2}}{g_{mMSF0}^2}\right) \tag{11}$$

$$\frac{\overline{dv_{1/f\_SF}^2}}{df} = \frac{K}{C_{OX}f}\left(\frac{1}{W_{MSF0}L_{MSF0}} + \frac{g_{mMSF1}^2}{g_{mMSF0}^2 W_{MSF1}L_{MSF1}} + + B^2\frac{g_{mMSF2}^2}{g_{mMSF0}^2 W_{MSF2}L_{MSF2}}\right) \tag{12}$$

where g_{mMSF0}, g_{mMSF1}, g_{mMSF2} are the transconductances of the MSF0-MSF2 transistors, W_{MSF0}, W_{MSF1}, W_{MSF2} are the widths of the MSF0-MSF2 transistor gates, and L_{MSF0}, L_{MSF1}, L_{MSF2} are the lengths of the MSF0-MSF2 transistor gates.

The presented mathematical terms show which parameter of the design has the major influence on the total input equivalent noise. Thus in order to reduce the input differential pair noise contribution (transistors M1 and M2) the large widths of transistors are preferred while the lengths should be chosen relatively small. Keeping in mind the matching requirements, the dimensions of the transistors M1 and M2 are set to W_{M1}/L_{M1} = 175 µm/0.5 µm. The source follower transistor MSF0 also has to be a part with a large transconductance and large area to reduce the 1/f noise. Finally the W_{MSF0}/L_{MSF0} ratio is equal to 350 µm/4 µm.

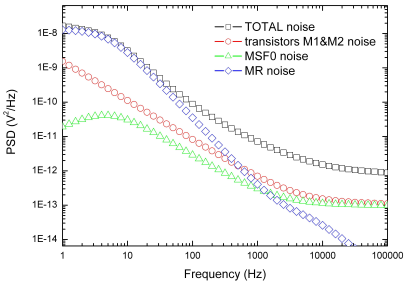


Fig. 4. Power spectral density simulation results of the main noise contributors on the preamplifier output.

Table 2. Percentage input referred noise contribution of the particular channel components.

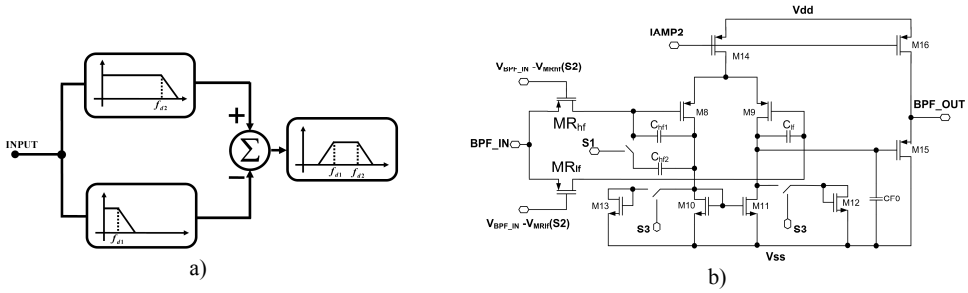
Component	Input Referred Noise Contribution [%]*
MSF0	1.6
MSF1	2.1
MR0	45
M1, M2	2 x 3.2
M3, M4	2 x 12.2

*- results were counted as a division of the square of the particular component's noise contribution and the square of the total input referred noise

The performed simulation shows that the main noise contribution originates in the preamplifier stage (80% of the overall input referred noise). Fig. 4 presents the power spectral density (PSD) of the most important components of the preamplifier. Table 2 summarizes the percentage noise contribution of these components to the total noise. Clearly, it may be noticed that the largest part of the noise comes from the input high pass filter.

2.4. Pass-band filter with frequency tuning

The band-pass filter operation is based on subtracting two signals filtered by the low pass filters with different cut-off frequencies f_{d1} and f_{d2}. As is shown below (Fig. 5 a), the result of such an operation is a band-pass filter with cut-off frequencies f_{d1} and f_{d2} [19]. The scheme of the filter core is shown in Fig. 5 b). The band-pass filter is obtained as a combination of two RC low-pass filters and a differential amplifier M8-M14.



a) b)

Fig. 5. Band pass filter: a) simplified block diagram, b) simplified scheme of the filter.

The resistors of the RC filters are built of transistor MR_{hf} of W_{MRhf}/L_{MRhf} = 10µm/30µm and transistor MR_{lf} of W_{MRlf}/L_{MRlf} = 1 µm/150 µm, both biased in the linear region. The input signal is applied simultaneously to the sources of these transistors and with a DC offset to their gates. The effective resistance of MR_{hf} transistor is about 700 kΩ while the MR_{lf} transistor resistance can be changed by the S2 switch (it can be either 80 MΩ or 800 MΩ). The effective capacitances are formed by the metal-insulator-metal capacitors C_{hf1} = 0.5 pF and C_{hf2} = 3.2 pF for the high cut-off frequency and by the C_{lf} = 8 pF for the low cut-off frequency (multiplied by the gain of the differential stage M8-M14 due to the Miller effect). The transfer function of the band pass filter is as follows [19]:

$$K_{tr}(s) \approx K_0 \frac{s(1-\frac{s}{z_2})}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})} \tag{15}$$

where K_0, z_2, $p_1$and p_2 are given by

$$K_0 = \frac{g_{mM9}}{g_{dsM9}+g_{dsX}}(C_{lf}R_{lf} - C_{hf}R_{hf}), \quad z_2 = -\frac{2g_{mX}(C_{lf}R_{lf} - C_{hf}R_{hf})}{C_{hf}C_{lf}(R_{lf}+R_{hf})}, \tag{16-17}$$

$$p_1 = -\frac{1}{\frac{g_{mM9}}{g_{dsM9}+g_{dsX}}C_{lf}R_{lf}}, \quad p_2 = -\frac{1}{C_{hf}R_{hf}}, \tag{18-19}$$

where g_{mM9} is the transconductance of the M9 transistor, g_{dsM9} is the source-drain conductance of the M9 transistor, C_{lf}, C_{hf} are capacitance values of corresponding capacitors in Fig. 5(b), R_{hf}, R_{lf} are resistance values of small-signal resistances of the MR_{hf} and MR_{lf} transistors.

The g_{mX} depends on the state of switch S3 and is equal to either $g_{mX}=g_{mM11}$ or $g_{mX}=g_{mM11}+g_{mM12}$, g_{dsX} depends on the switch S3 state and is equal to either $g_{dsX}=g_{dsM11}$ or $g_{dsX}= g_{dsM11}+g_{dsM12,}$ C_{hf} depends on switch S1 and is equal either $C_{hf}=C_{hf1}$ or $C_{hf}=C_{hf1}+C_{hf2}$.

There are three different switches to control the cut-off frequencies in the filter stage:

- S1 to modify the effective value of C_{hf} capacitance and S2 to change the small signal resistance mainly of MR_{lf},
- S3 to change the effective gain of differential amplifier M8-M14 and in this way to alter the multiplication factor for the Miller effect.

The band pass filter consumes 20 µW of power and its gain is 0.7 dB. The parameters of its main components are presented below (see Table 3).

Table 3.Parameters of the main components of the band pass filter.

Component	Parameter	g_m/I_d [V^{-1}]	Operating Region
MR_{hf}	10 µm/30 µm	-	SI
MR_{lf}	1 µm/150 µm	-	WI
M8, M9	1000 µm/0.5 µm	26.5	WI
M10, M11	192 µm/21 µm	21	MI
M12, M13	30 µm/25 µm	21.1	MI

2.5. Analog multiplexer and digital noise minimization

In order to reduce the number of output lines, the 64 analog signals from the 64 front-end channels are multiplexed to a single output by an analog multiplexer. The block diagram of the multiplexer is presented in Fig. 6. The multiplexer is built of 64 channels consisting of sample and hold circuit and input buffers. The multiplexer is controlled by three external digital signals:HOLD_ALL, CLOCK and RESET. All of them are applied in the differential mode using the LVDS levels to reduce the pick-up of digital noise by the sensitive analog circuits. During the sequential readout of the hold capacitors (CH0-CH63), the transmission gate of TGSD is switched on and the signal from the dummy channel is subtracted from the signal value from other channels in the DIFF block. This helps to reduce the injection of power supply and clock related noise into the signal path.

The bandwidth of a single channel is limited to 15 kHz. The nominal frequency of multiplexer operation is 5 MHz what results in an approx. 75 kHz sampling frequency per single channel and it is enough to avoid the aliasing problem.

For test purposes the readout of the multiplexer can be performed in two ways, either all channels are read sequentially or only one channel is read continuously.

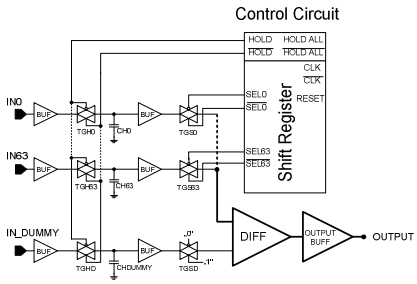


Fig. 6. Simplified scheme of the multiplexer.

3. Test results

In order to perform measurements of the functionality of the integrated circuit it was bonded to the prototype 6-layer PCB equipped with a TTL to LVDS converter and a socket for 60-channel specimen slides used for extraction of information from electrically active tissue slices and cell cultures. For the multiplexer data acquisition a PXI (PCI eXtensions for Instrumentation) module has been used, equipped with high-speed analog/digital output card (NI-PXI 6733) and a 100 MS/s, 14-Bit Digitizer (NI-PXI 5122). An output card serves as a source of multiplexer control signals (CLK, RESET, HOLD_ALL) and a source of input test signals for analog channels. The digitizer acquires the output signal for further processing i.e. decimation and demultiplexing.

3.1. Pass-band settings

The pass-band of a single channel can be changed by tuning of the time constant in the AC-coupled input stage and by the switches in the filter stage (S1, S2, S3). Using the analog control at the input (VG voltage - see Fig. 2) the low cut-off frequency can be tuned continuously from 1 Hz to 60 Hz as it is shown in Fig. 7(a). The high cut-off frequency can be changed only by switches in the filter stage, setting its value in steps around 3.5 kHz, 9 kHz or 15 kHz (see Fig. 7(b)). The frequency tuning allows to find the best settings for given neurobiological tests, however it influences the noise performance and signal to noise ratio in our system.

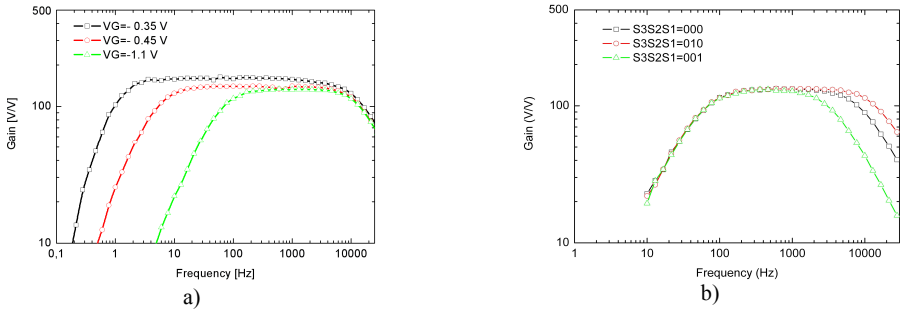


Fig. 7. Measured frequency response of a single channel for: a) tuning the time constant of the input AC-coupled circuit, b) different values of switches S1, S2, S3 to change the high cut-off frequency.

3.2. Channel-to-channel uniformity

The ASIC consists of 64 identical channels with the bias and control currents common for all the channels. Therefore, the spreads of the basic parameters from channel to channel, like gain, output offsets, cut-off frequencies, are important having in mind single ASIC applications and also future large multi-chip systems. Typical distributions of these parameters measured for the ASIC are shown in Fig. 8 and Fig. 9. The spread of the gain defined as standard deviation to mean value (sd/mean) is equal to 4.4%. The low offset spread at the multiplexer outputs (standard deviation is equal to 3.5 mV) makes the future operation with external ADC much easier.

Probably the most difficult parameter in many of the multi-channel ASIC designs for neurobiology experiments is the small spread of the low cut-off frequency from channel to channel. For our design this spread is on the level of 4.4% - see Fig. 9(a). The spread of the high cut-off frequency is about 1.8% - see Fig. 9(b).

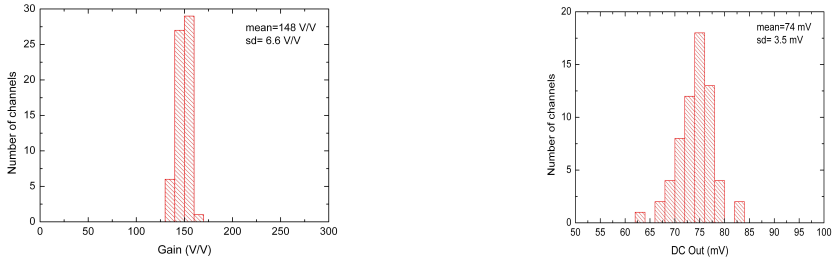


Fig. 8. Spread of analog parameters in 64-channel ASIC: (a) gain, (b) output offset.

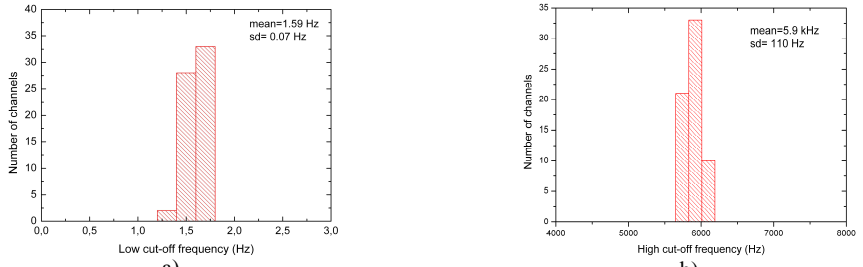


Fig. 9. Spread of analog parameters in 64-channel ASIC: (a) low cut-off frequency, (b) high cut-off frequency.

Another aspect of such designs is the yield of working channels versus the main parameters. Since the crucial parameter of such applications is the low cut-off frequency, we made measurements showing the yield of working channels versus the low cut-off frequency. In order to change the low cut-off frequency one may use the VG input (see Fig. 2). It changes the gate source voltage of the MR0 transistor resulting in its different resistances. Despite the possibility of changing low cut-off frequencies, transistor MR0 plays a second role – it biases the inputs of the differential amplifier. Thus it may limit the number of working channels and influence the spread of the low cut-off frequency. Table 4 shows the number of working channels in 64 channel ASIC versus the low cut-off frequency setting.

Table 4. Exemplary results of the spread of the low cut-off frequency (S3S2S1=001).

VG – V_{INREF} [V]	Low cut-off frequency [Hz]	Spread of the low cut-off frequency (sd/mean) [%]	Number of working channels
-1.1	59.6	2.2	64
-0.9	43.3	1.8	64
-0.7	26.6	1.8	64
-0.5	8.58	2.3	64
-0.4	2.62	3	64
-0.37	1.59	4.4	63
-0.35	1.06	10.3	61
-0.3	0.53	83	56

Since the VG input controlling the resistance of the MR0 transistor is common for all the channels and there is a spread of the threshold voltage of this transistor, it is difficult to operate with all channels in the frequency range below 1 Hz. However, we checked experimentally that setting the low cut-off frequency at the level of 0.5 Hz is possible for each channel but this requires an additional correction DAC for controlling the VG voltage individually in each channel. Such solution we utilize in our other ASICs, for example [17, 18] and it will be also used in the next version of this one.

3.3. Noise measurements

We measured the noise of the ASIC for different values of cut-off frequencies in the filter stage and different time constants of the input AC coupling circuit. The examples of measured Power Spectral Density (PSD) of noise for two different pass-band settings are shown in Fig. 10:

- setting I: pass-band 20 Hz - 6.5 kHz, gain 42 dB,
- setting II: pass-band 1 Hz - 13 kHz, gain 44 dB.

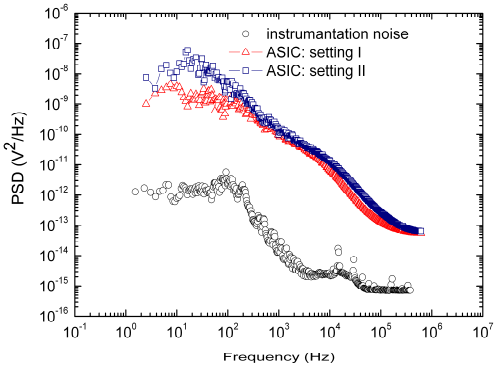


Fig. 10. Power spectral density of output noise of an ASIC (for two different settings of the band-pass filter) and of instrumentation noise.

Taking the square root of integrals from plots in Fig. 10 and dividing these results by the gain of the circuit, one can obtain the rms value of equivalent input referred noise, which is equal to 6 μV rms and 11 μV rms respectively. The considerable part of the total input referred noise originates in the dummy channel (about √2 of a single recording channel) which in the future system will be optional. Taking into account the noise contribution of the measuring probes, the noise of our system is low enough for most of neurobiological

experiments. Thanks to different test structures implemented in our ASIC, the effect of higher noise is the subject of our intensive investigations.

4. Neurobiology experiments

The presented ASIC was employed in a system dedicated for in vivo experiments. The system consists of the presented ASIC bonded to the PCB module which is combined with the 64 channel electrodes provided by Neuronexus Technologies (see Fig. 11(a)). The experiment was performed on a rat under urethane anaesthesia at the Department of Neurophysiology and Chronobiology, Jagiellonian University in Cracow, Poland. The electrodes were implanted into the brain to record infraslow oscillations at the level of neuronal spiking in the intergeniculate leaflet of the rat lateral geniculate nucleus [20]. Signals from 64 channels were recorded for a few hours and the results from selected channels with the neuronal spiking are shown in the Fig. 11(b).

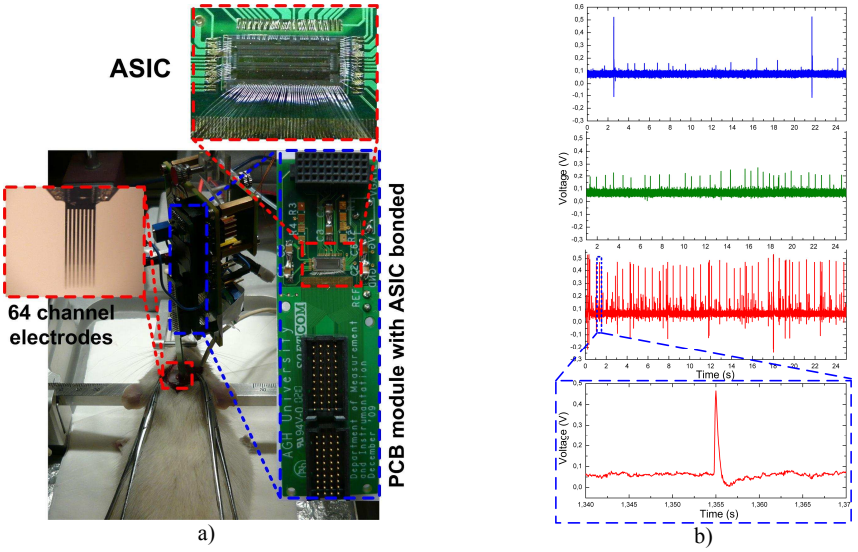


Fig. 11. (a) Photo of 64 channel system for in vivo experiments, (b) Neuronal spikes at the output of three exemplary ASIC channels.

5. Conclusions

We have shown novel solutions of a low-noise multi-channel integrated circuit working in the low frequency range and realized in CMOS 180 nm technology.
There are many works presenting multichannel integrated circuits dedicated to neurobiology experiments, however a known problem is the small spread of low cut-off frequency. Table 5 presents the papers which discuss this problem and shows the spread of their corner frequencies. To our knowledge the ASIC presented in this paper is the first solution which allows to obtain a low cut-off frequency in the range of about a single Hz with all the channels working at the same time. The low noise performance of the IC, small power consumption and good channel-to-channel matching make the ASIC an universal multi-channel readout integrated circuit for experiments with live neuronal cells. This ASIC can be used in systems comprised of several hundreds/thousands of readout channels for both in vivo and in vitro experiments. The modern CMOS 180 nm process used in our design guarantees

that additional chip functionality (like wireless link, ADC or data compression) can be relatively easily implemented.

Table 5. Comparison of published, front-end amplifiers for multichannel neural recording.

Parameter	[14]	[9, 21]	[19]	**This work**
Number of channels	64	16	64	**64**
Technology	CMOS 0.5 µm	CMOS 0.35 µm	CMOS 0.7 µm	**CMOS 0.18 µm**
Gain [dB]	60	34	40 - 60	**44**
Tuning range for low cut-off frequency	12 Hz – 112 Hz	2 Hz – 300 Hz	10 Hz – 130 Hz	**1 - 60 Hz**
Tuning range for high cut-off frequency	50 Hz – 4.5 kHz	3.3 kHz	400 Hz – 2.8 kHz	**3.5 kHz - 15 kHz**
Equivalent input noise	3.1 µV	3 µV	3 µV	**6 µV**
Power per channel	2000 µW	100 µW	1700 µW	**220 µW**
Spread of low cut-off frequency	1.8 %	40 %	9.8 %	**4.4 %**
Spread of high cut-off frequency	1.7 %	2.4 %	0.86 %	**1.8 %**
Spread of gain	1.7 %	0.8 %	1.2 %	**4.4 %**

Acknowledgements

This research and development project was supported by the Polish Ministry of Science and Higher Education in the years 2008-2010 (NR 01-0011-04/2008).

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